Hall Ticket Number:

Code No. :14416 N/O

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

B.E. (ECE: CBCS) IV-Semester Main & Backlog Examinations, May-2019

Pulse, Digital and Switching Circuits

Time: **3** hours Max. Marks: **60**

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** from **Part-B***

Q. No.	Stem of the question	M	L	CO	PO
	Part-A (10 × 2 = 20 Marks)				
1.	List any two applications of clippers and clampers.	2	3	2	1
2.	Define an attenuator. What is the need of compensating an attenuator?	2	1	1	1
3.	A Schmitt trigger circuit is designed with UTP and LTP as 2V and 1V respectively. Draw the output waveform of Schmitt trigger circuit for input of $3\sin(\omega t)$.	2	3	3	2
4.	Define transmission error of a sweep signal and give its expression.	2	2	3	1
5.	Prove the following identity: XY+X′Y′+YZ = XY+ X′Y′+X′Z	2	3	4	2
6.	Distinguish between prime implicant and an essential prime implicant?	2	4	4	1
7.	Illustrate static-0 hazard with an example.	2	2	4	1
8.	Explain the Race around condition. How can it be avoided?	2	2	4	1
9.	Draw the state diagram of T flip-flop	2	3	4	3
10.	What is One hot encoding and give its importance.	2	2	5	1
	Part-B (5 × 8 = 40 Marks)				
11. a)	Derive the expression for percentage tilt of RC high pass circuit for a square wave input.	4	2	1	2
b)	Design a diode clamper to restore the positive peaks of 1KHz input signal to a voltage level of 5V. Assume $R_f = 200\Omega$, $R_r = 500K\Omega$ and the voltage drop across the diode as 0.7V.	4	4	2	3
12. a)	Design a collector coupled monostable multivibrator for a pulse width of 1ms.Assume all saturation voltages of transistor as zero, $V_{CC} = -V_{BB} = 12V$,$V_{BE(cutoff)} = -2V$,$I_{C(sat)} = 10mA$, $h_{FE} = 40$ and $I_{B(sat)} = 1.5 \times I_{B(min.)}$.	4	4	3	3
b)	Explain the working of Sweep Circuit using UJT with the help of circuit diagram.	4	1	3	1
13. a)	Implement the two input Ex-OR operation using only two input NAND gates without using complemented variables.	3	2	4	2
b)	Simplify the following Boolean function by using Quine-McCluskey method $f(A,B,C,D) = \sum m(0,2,3,6,7,8,10,12,13)$	5	2	4	2

Contd…2

14. a)	Design a code converter, which can convert a 4-bit BCD into a 4-bit Excess-3 code.	4	4	4	3
b)	Draw the circuit diagram of a Master-Slave J-K flipflop and explain its need and operation with the help of truth-table.	4	2	4	1
15. a)	Construct a four-bit Johnson counter and explain its operation.	4	2	4	1
b)	Design a sequence detector circuit, which detects three or more consecutive 1's in a string of bits coming through an input line. i) Find the state diagram ii) Determine the type of the circuit (Moore or Mealy model) .	4	5	5	4
16. a)	Describe the operation of negative peak clipper with and without reference voltage.	4	2	2	1
b)	Design a collector coupled Astable multivibrator for a duty cycle of 40% and output frequency of 1.5KHz. Assume all saturation voltages of transistor as zero, V_{CC}=12V ,h_{FE}=40 ,$I_{C(sat)}$=5mA and $I_{B(sat)}$ =1.5×$I_{B(min.)}$.	4	4	3	3
17.	**Answer any *two* of the following:**				
a)	Expand the following expression into canonical SOP and canonical POS forms: f(A,B,C,D) = (A+D′)(A+C′)(A′+B)(A′+B+C)	4	2	4	2
b)	Realize the following Boolean function, F(A,B,C,D) =∑m(1,2,4,7,9,10,12,14,15) using 8:1 Multiplexor.	4	3	4	3
c)	Describe the operation of Parallel-in Serial-out shift register in detail.	4	2	4	2

M: Marks; L: Bloom's Taxonomy Level; CO: Course Outcome; PO: Programme Outcome

S. No.	Criteria for questions	Percentage
1	Fundamental knowledge (Level-1 & 2)	58
2	Knowledge on application and analysis (Level-3 & 4)	37
3	*Critical thinking and ability to design (Level-5 & 6) (*wherever applicable)	5

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